WHAT IS CLAIMED IS:

1. A circuit comprising:

two voltage sources; and

a switching structure having a first terminal coupled to an output of a first voltage source and a second terminal coupled to an output of a second voltage source, the switching structure containing circuitry to electrically couple the outputs together based on a value on a control signal line.

2. The circuit of claim 1, wherein when the switching structure is off, then the outputs are decoupled.

3. The circuit of claim 1, wherein each of the two voltage sources produce an output of equal voltage potential.

4. The circuit of claim 1, wherein the switching structure is a transistor, the first terminal is the transistor's source, and the second terminal is the transistor's drain.

5. The circuit of claim 4, wherein the control signal line is coupled to the transistor's gate.

6. The circuit of claim 4, wherein the transistor is a P-type MOSFET (metal oxide semiconductor field effect transistor).

7. The circuit of claim 4, wherein the transistor is an N-type MOSFET (metal oxide semiconductor field effect transistor).

8. The circuit of claim 4, wherein the transistor is made from thick oxide to provide low-leakage characteristics.

9. The circuit of claim 1, wherein the voltage sources are used to power separate power domains.

10. The circuit of claim 1, wherein the voltage sources are used to power sub-domains within a single power domain.

11. The circuit of claim 1, wherein each of the two voltage sources comprises a voltage supply controlled by a switch.

12. The circuit of claim 11, wherein the switch in each voltage source is a transistor, wherein the switching structure is a transistor, and wherein the width of the transistors in each voltage source are approximately equal and the width of the transistor in the switching structure is on the order of 10 to 20 percent the width of the transistors in the voltage sources.

13. The circuit of claim 12, wherein the voltage source transistors and the switching structure transistor are P-type MOSFETs (metal oxide semiconductor field effect transistor).

14. The circuit of claim 12, wherein the voltage source transistors and the switching structure transistor are N-type MOSFETs (metal oxide semiconductor field effect transistor).

15. The circuit of claim 1, wherein the voltage sources share a common voltage supply.

16. The circuit of claim 1, wherein each voltage source has an independent voltage supply.

17. The circuit of claim 1, wherein the switching structure reduces turn on current spikes.

18. A circuit comprising:

M voltage sources, wherein M is an integer number greater than two (2); and

a switching network having M terminals, wherein each terminal is coupled to an output from one of the M voltage sources, the switching network containing circuitry to electrically couple the outputs of the M voltage sources, wherein the coupling of the outputs is based on a mapping.

19. The circuit of claim 18, wherein some of the voltage sources produce outputs with the same voltage potential.

20. The circuit of claim 19, wherein the outputs of voltage sources coupled together all have the same voltage potential.

21. The circuit of claim 19, wherein switches couple the outputs, and wherein outputs with different voltage potentials are not connected by switches.

22. The circuit of claim 18, wherein the mapping is stored in a memory.

23. The circuit of claim 18, wherein the mapping is dynamically computed.

24. The circuit of claim 18, wherein switches couple the outputs, and wherein the mapping specifies the state of each switch in the switching network.

25. The circuit of claim 18, wherein each output is connected to each other output via a switch.

26. The circuit of claim 18, wherein each output is connected to two other outputs via a switch.

27. The circuit of claim 26, wherein the outputs are connected in a circular fashion.

28. The circuit of claim 18, wherein the M voltage sources supply power to M power domains.

29. The circuit of claim 18, wherein the M voltage sources supply power to M power sub-domains within a single power domain.

30. The circuit of claim 18, wherein the switching network comprises a plurality of switching structures, each switching structure coupling two outputs of equal voltage potential together, the switching structure comprising:

a first terminal coupled to an output of a first voltage source;

a second terminal coupled to an output of a second voltage source; and

the switching structure further comprising circuitry to electrically couple the outputs together based on a value on a control signal line

31. The circuit of claim 30, wherein the switching structure is a transistor, the first terminal is the transistor's source, the second terminal is the transistor's drain, and the control signal line is coupled to the transistor's gate.

32. An integrated circuit comprising:

a circuitry block; and

a plurality of power supplies, each coupled to the circuitry block, each power supply comprising:

M voltage sources, wherein M is an integer number greater than one (1); and

a switching network having M terminals, wherein each terminal is coupled to an output from one of the M voltage sources, the switching network containing circuitry to electrically couple the outputs of the M voltage sources, wherein the coupling of the outputs is based on a mapping.

33. The integrated circuit of claim 32, wherein the circuitry block comprises a plurality of circuit blocks, and wherein there is at least one power supply associated with each circuit block.

34. The integrated circuit of claim 33, wherein all power supplies are identical.

35. The integrated circuit of claim 33, wherein each power supply may be designed differently.

36. The integrated circuit of claim 33, wherein each circuit block and its associated power supply are located adjacent to one another on the integrated circuit.